LC & LRT SERIES

RADIO TRANSMITTERS, RECEIVERS & TRANSCEIVER MODULES & PIC CONTROLLERS/MODEMS

LC450, LC869, LRT170 & LRT470

Version1.1 23/01/02

Contents

1.0 INTRODUCTION

1.1 MANUAL INFORMATION

This document covers the LC & LRT radio modules and is a step by step guide on how to integrate the modules and associated circuitry into your application. It caters for the competent engineer requiring a quick radio solution. If a less integrated solution is required, then the QRT PCB with the LC or LRT and RS232/5VTTl or Audio interface is available, brief details are included in section 4.

Should the manual be insufficient, further information and help can be obtained from our technical department.

1.2 PRODUCT OVERVIEW

1.2.1 TRANSCEIVER, TRANSMITTER or RECEIVER CONFIGURATIONS

The LC & LRT can be ordered as a Transceiver, as a Receiver (A transceiver, with the transmitter part unpopulated), or as a Transmitter (A transceiver, with the receiver unpopulated).

1.2..2 LC450 & LC869

The LC450 & LC869 are very low cost, low current consumption 500mW (5mW – 750mW) transceivers for use in the licensed exempt telemetry & data market. The product has been designed to meet the requirements of ETS300-220/UK MPT1329 & ETS301-499 (CE) or equivalent specifications.

1.2.3 LRT470 & LRT170

The LRT & LC modules are physically the same size, shape and have the same pin configuration enabling either to be used in the same in application. The LC series is a single board construction with a solder-in VCO, whereas the LRT has daughter boards for the antenna filter and RF power amplifier. The LRT can be ordered with either a low power
(5mW – 750mW) or high power (50mW- 5watt) RF power amplifier. The 5watt version will require additional heat sinking. The LRT modules were designed primarily for licensed applications requiring testing to ETS300-113, 086, MPT1411 (VNS2111) and ETS301-489.
Hence, the receiver has an improved specification to enable it to meet the relevant requirements. As a consequence the current consumption on receive is about 5mA higher than the LC.

1.3 RF POWER CONTROL

The LC & LPR series have an internal and external RF power control. The internal is adjusted by a pre-set potentiometer, or the power control can be controlled externally by a control voltage from a potentiometer or MPU.

1.4 RECEIVED SIGNAL STRENGTH (RSSI)

The RSSI output voltage is available as a 0-5VDC level, relative to the received signal strength. This voltage can be used to decide if the link path is acceptable.

1.5 MODULATION & DATA INTERFACE

A DC input & output path is provided to the transceiver to accommodate various forms of modulation. However, for optimum performance the PIC Modem (available from R.F Technologies) with its selectable baud rate is recommended.

1.6 CONSTRUCTION

The LC/LRT are PCB mount RF modules with a screening can to prevent interference
in either direction. The radio is a complete RF solution and was designed to interface with a microprocessor or a pre-programmed PIC Modem, with baud rates & channels selected via a

suitable switches or by external control. Information on synthesizer loading and control software for the product is detailed in this manual. Pre-programmed PIC's or PIC Modems may be purchased from R.F Technologies.

1.7 PIC MICROPROCESSOR CONTROLLER & SOFTWARE

For simple applications where the unit will be externally modulated, a PIC controller is recommended, a workable software listing is shown as an example in section 3.
Alternatively pre-programmed PIC's can be obtained from the sales office.

1.8 PIC MODEMS

RFDataTech have developed "Softmodem" Technology, which is to say we use the PIC as a DSP device and encode/decode FSK, FFSK & GMSK within the PIC controller.
This makes for a very low cost, low power integrated solution with a programmable baud rate of 150 – 4800bps. An example of the protocol to talk to the PIC Modem is outlined in section 6.

1.9 COMPETE QRT PRODUCT BASED ON THE LC & LRT

For a complete solution, with an RS232 or 5VTTL interface, we recommend the QRT Series. These are LC & LRT modules mounted on control & interface boards which have programmable modems and audio paths and are ready to use. These can be provided as PCB assemblies or complete products mounted in an enclosed tough milled aluminum enclosure. For further information look at the QRT documentation. A drawing of the enclosure is shown in section 4

1.10 ENCLOSURES

Should your applications require low cost aluminium enclosures, we can supply the QRT extruded enclosures machined to specification at a nominal cost.

2.0 TECHNICAL SPECIFICATIONS

2.1 GENERAL

Frequency Range:	LRT	150 - 170MHz
	LC & LRT	406 - 475MHz
	LC	868 - 870MHz
Channel Spacing:	12.5KHz (optional 20/25/30KHz)	
	LC869 25KHz	
Number of Channels:	Any number within the programmable bandwidth	
Power Requirements:	LRT 5Watt	8V
	LC/LRT 1Watt	5V DC
Operating Temp:	-30deg C to +60Deg C.	
Humidity:	0 - 95% Non-Condensing	
Frequency stability:	<2.0ppm -25deg C to +60deg.C	
Size:	78 x 52 x 19mm	
Weight:	150gms	

Connectors:	Interface	15 way 0.1pitch pins with mating sockets supplied
	Antenna	LRT 50 ohm MCX LC Coax cable or optional MCX socket

2.2 TRANSMITTER

RF Power:	LPR/LC -1	5mW – 750mW.
	LPR-5	50mW - 5Watts
Output Impedance:	50 ohms	
Programmable Bandwidth:	900MHz	15MHz within the F band without re-alignment
	UHF	10MHz within the F band without re-alignment
	VHF	5MHz within the F band without re-alignment
Audio Input:	1V P-P	
TX Keying:	GND to enable	
Deviation:	± 7.5KHz Max.	
Adj. channel power:	Better than 65dB	
Spurious emissions:	< 0.25µW (4nW within specified bands)	
Rise time:	Cold Start	< 20mS
	From Standby	< 10mS

2.3 RECEIVER

Sensitivity:	Better than 0.25µV (-119dBm) for 12dB SINAD phosphormetricly weighted	
Programmable Bandwidth:	UHF	10MHz within the F band without re-alignment
	VHF	5MHz within the F band without re-alignment
Spurious & Image response:	LRT Series	75dB
	LC Series	68dB
Blocking:	>LRT	90dB relative to 1µV
	>LC	85dB

Intermodulation:	>LRT Series 65dB >LC Series 60dB
Adjacent channel:	>LRT Series 65dB at 12.5KHz >LC Series 60dB at 12.5KHz
IF frequencies:	45MHz and 455KHz
External Audio Output:	LRT 300mV rms LC 150mV rms
Mute response time:	<3msec
Received Signal Strength (RSSI):	Range -120dBm to -40dBm

2.4 OPTIONAL SOFTMODEM PIC

Standard Signaling formats:	PICM1; 150 – 2400 FFSK programmable V23 or Bell 202, NRZ or NRZI up to 1200 baud, inverted or true, 2400 baud uses fixed NRZI format coherent 1200/2400Hz. PICM2 includes 4800 GMSK.
Optional Signaling formats:	512, 1200, 2400 POCSAG, 2 tone & 5 tone EIA, ZVEI, CCIR etc.
Interface:	2Wire serial 5V TTL with serial baud rate 1200, 2400, 4800 or 9600bps.

Bit Error Rates (BER): 2400 FFSK 1 x 10-3 @ -118dBm

In the interest of improvement, the above specifications are subject to change without notice.

3.0 APPROVALS

The LC & the LRT modules have been tested in conjunction with the PIC/M1 & M2 modem controllers & associated circuitry as described in this document in various products designed by ourselves and others. All the products have been tested and meet the relevant specifications outlined in 3.5.

3.1 Modulation:

To cater for various clients' modulation requirements, the modulation input is DC coupled and has no on-board filtering. Hence, a splatter filter (low pass filter) will be required to limit the maximum frequency and remove harmonics. The circuit in section 7 can be used or others can be configured. Testing should be performed to prove the effectiveness of any filter to reduce the adjacent channel interference.
Should help be required, we can test the filters performance at our offices.

3.2 Transmitter Rise & Fall :

For ETS300-113 & 086 the rise and fall of the transmitter must be controlled to limit transient responses (Key-up Splashes) the rise and fall is controlled by internal circuitry within the module and does not require any external ramping.

3.3 Screening:

The screening on the LC & LRT is designed to keep spurious radiation and harmonics in and keep out possible interfering signals from associated circuitry and microprocessors.

The LC meets the requirements of ETS300-220 & ETS301-489 without additional screening, provided the pin decoupling is adhered to.

The LRT 5watt module may need some additional screening in the form of a sprayed plastic or metal enclosure as leakage may occur around the PA Block.
From our experience only very nominal additional screening is required.

3.4 Testing:

Although the product meets the requirements of the specifications below, once included on a clients PCB, Testing to CE (ETS301-489) of the complete unit is normally required. With the exception of the CE testing, RFDataTech can check out the radio's performance within your product, at our labs.

3.5 Specifications:

The LC & LRT have been tested and comply with the following specifications.

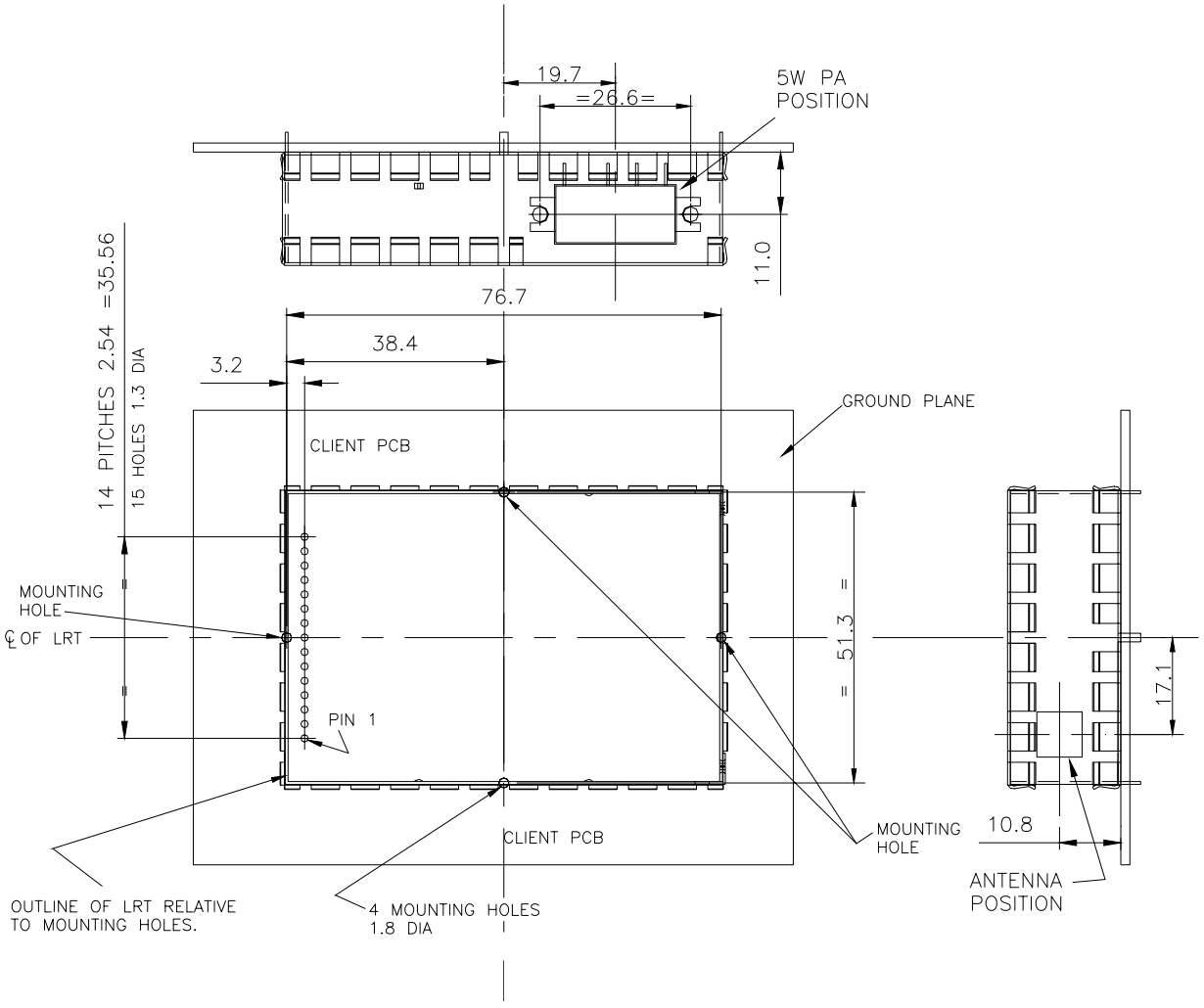
LC450 & 869 Transmitter, Receiver & Transceiver
ETS300-220 & ETS301-489

LRT470 & 170 Transmitter, Receiver & Transceiver
ETS300-220, 113, 086 & ETS301-489

4.0 APPLICATION

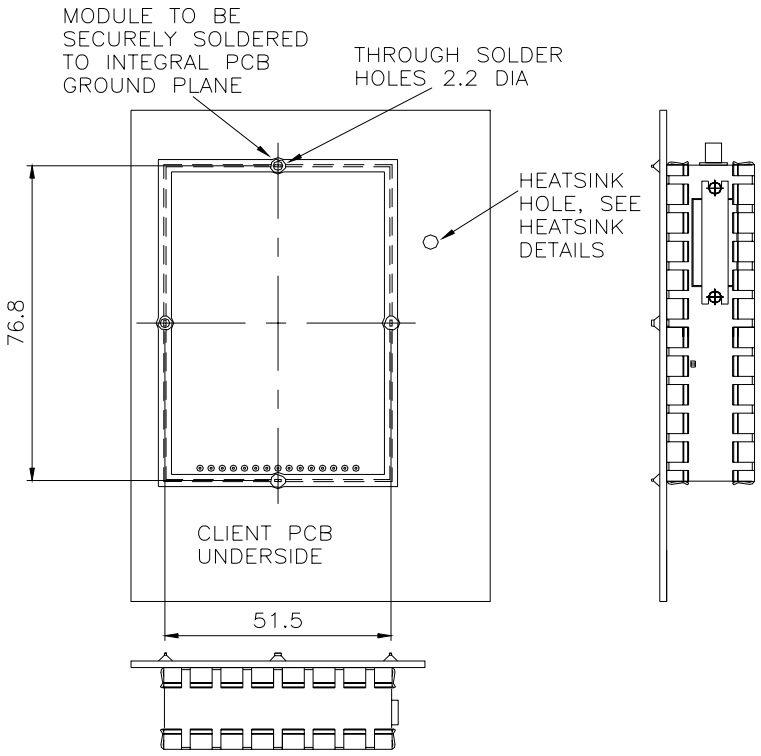
4.1 DIMENSIONS & MOUNTING

The drawing below shows the mechanical size of the module and PCB layout in order to mount the product. The interface to the LRT & LC products is via a 15 way gold plated 0.1 pitch, single in line, plug. The mating half, for PCB mounting is supplied with the product. The drawing shows the location of the 5Watt PA block used on the higher power modules,
for the low power versions, ignore the block.



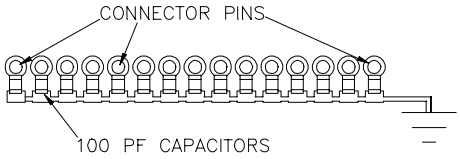
4.2 MOUNTING & EARTHING

The LRT & LC should have continuous earthing between the mounting points on at least one side of the PCB. The lower part of the module is supplied with an insulator so tracks can run under the module. Provided the earthing is good parts may be mounted under the model.



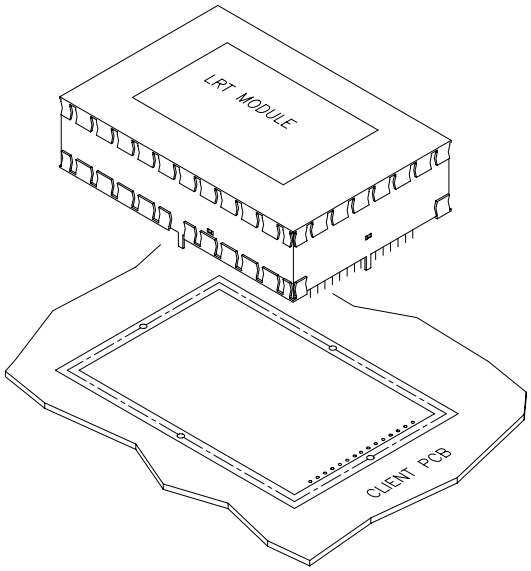
4.3 INTERFACE DE-COUPLING

We suggest the I.O pins are de-coupled with 100pf surface mount capacitors to ensure noise from external circuits does not interfere with the LPR module. If problems occur a 1nf may be used instead or put in parallel, however, care should be taken as additional loading of the synthesizer control lines may slow down the loading procedure, with a 1nf & 100pf the maximum suggested speed is 50K baud.
The 7.2 & 5VDC DC voltage pins will require 0.1uF as a minimum.



4.4 1WATT PCB MOUNTING DETAILS

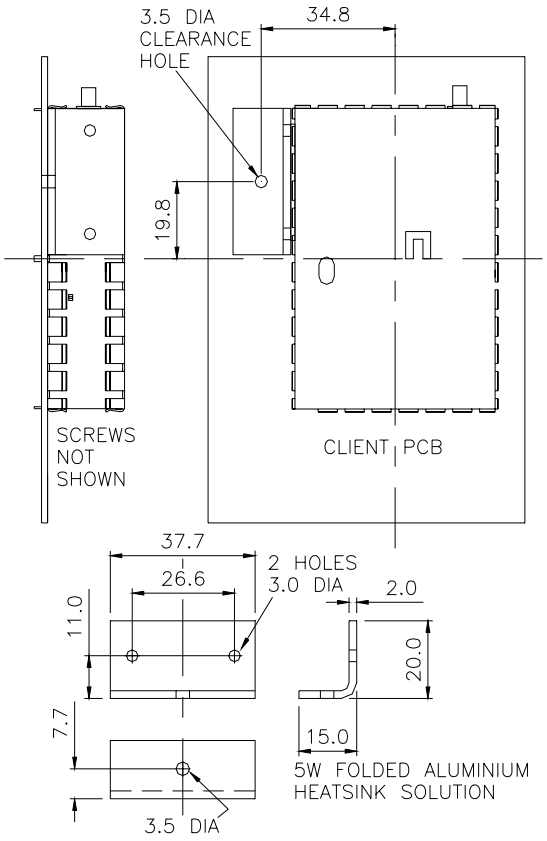
The 1 watt product requires no additional heat sinking when operated within the temperature range -25 to +60 deg.C.



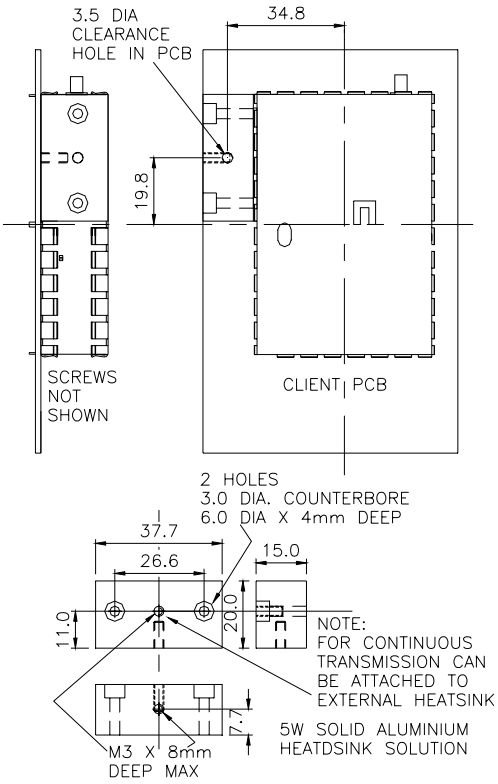
4.5 HEAT SINKING FOR 5WATT LRT's

The 5Watt product is supplied without a heat sink but will require one for operation.
The type of heat sink will depend upon the transmit duty cycle of the product.
For intermittent outstation applications a simple piece of right angle aluminum will suffice, but for very high transmit duty cycles a machined piece of aluminium may be required, that could be attached to a metal case or external heat sink. In all applications the heat sink should be connected to ground close to the module

4.5.1 Folded Aluminium Heat sink



4.5.2 Machined Aluminium Heat sink



4.6 LRT & LC PIN DESCRIPTION

All measurements taken from a standard production samples setup for 12.5KHz channel spacing, but there may be some slight variation.

PIN	Name	Description
1	**RXAUD**	The Audio Output from the receiver has an output Impedance of approximately 330 ohms. Output Level: LC Series approx. 300mV rms LRT Series approx 150mV rms Both outputs are for a modulating frequency of 1KHz with 1.5KHz of deviation.
2	**RSSI**	The Received Signal Strength Indication produces a voltage in the range 0-5VDC that is proportional to the received signal strength and is normally used to decide if the radio path will work. Output level 0– 5VDC LC Series –119dBm = 1.3VDC -80dBm = 2.6VDC LRT Series –119dBm = 1.1VDC

-80dBm = 1.99VDC

3 BUSY

This output switches between 0 & 5VDC when there is a signal present at a level greater than the internal mute setting. The signal can be used to wake up a microprocessor or other circuitry, on reception of a signal.
The output is low (0VDC) when the product receives a signal & sits at 5Volts when there is no signal.
Unless otherwise specified the mute is factory set for 12dB SINAD.

4 GND

Ground Connection

5 RADEN

The RADEN is used as a low current ON/OFF switch only on the LRT 5Watt product to avoid having to switch 8Volts at a high current for power save applications.

Open Circuit; The Radio operates
Connect to GND; Disables the radio.

RADEN is not used (the pin is N/C) on the LC Series & the 1Watt LRT as the relatively low current 5VDC supply can be switched externally for power saving.

6 TXP

Transmitter's RF Power Control
If the internal TX power Adjustment link is fitted (see TX power Section) applying 5Volts DC during transmit will produce the an RF power to the set level.
If the link is not fitted and then an external 0 – 5VDC, will produce a proportional RF output power.
The input has a low pass filter making it suitable for PWM operation via a MPU. In receive mode the pin should set to 0VDC.
For further information see the TX power section

7 TXAUD

Transmitter's modulation input & RX/TX frequency control point.
The modulation point is DC coupled and can be used to trim the frequency of the product. The modulation signal should be superimposed on a DC level of 2.5V (half rail point). There must be no signal present during receive.
The modulation sensitivity is 180mV for the LRT Series & 230mV for the LC Series.

8 GND

Ground Connection

9 TXSH

The Transmitter Shift switches in and out the TX & RX VCO's during their respective modes of operation.
OV (GND) Transmit
Open Circuit Receiver

10 PTT

Transmit Enable (Press To Talk)
Used to control the pin diode antenna switch
OVDC = Transmit
Open Circuit = Receive

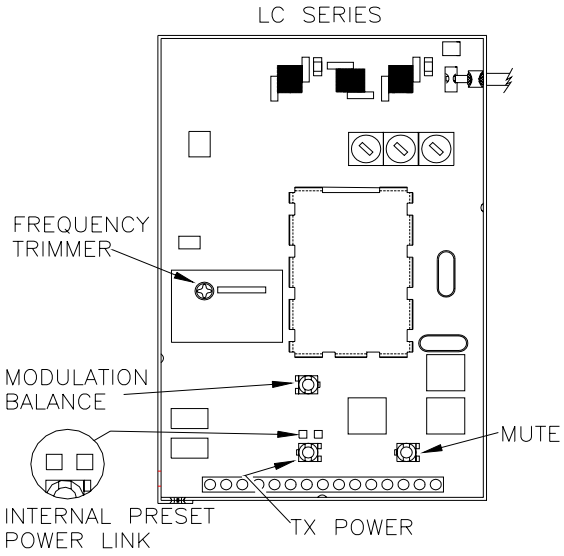
11	**CLK**	Synthesiser Clock Input High Impedance CMOS input, See synthesizer loading section & the National LMX2316 data sheet
12	**DATA**	Synthesiser Data input See the synthesizer loading section and the National LMX2316 data sheet
13	**EN**	Synthesiser Load Enable See the synthesizer loading section and the National LMX2316 data sheet
14	**LOCK**	Synthesiser Lock signal 0 = Out of Lock 5V = Locked
15	**+VDC**	Power Supply input (See Power Supply Section) Receive Mode approx 25mA LC & 1Watt LRT 5VDC (See Note 1) TX 700mW full power LRT 5Watt 8VDC 2Amps full power
ANTENNA		The LRT uses a MCX female connector The LC has a length of RG173 attached or can be supplied with an MCX female in-line socket.

4.7 POWER SUPPLY REQUIREMENTS:

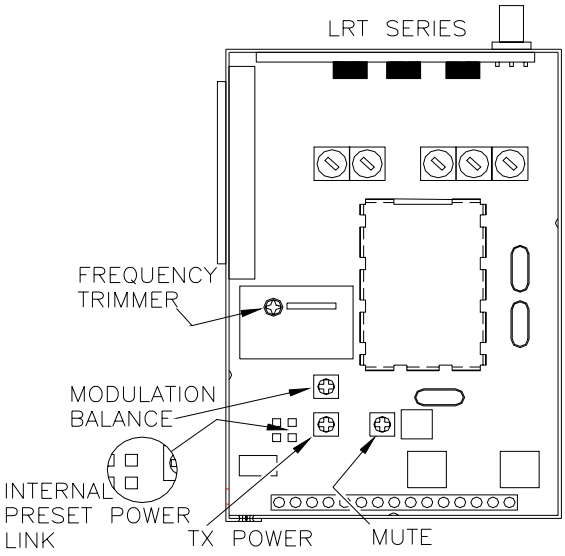
The LC & the LRT requires stabilized power supplies to operate,
The LRT 5Watt product operates from an 8VDC supply and has an internal 5Volt regulator the receiver & low power parts of the transmitter. The LC & the LRT operate directly from an external 5VDC supply that supplies the VCO & VCTCXO. Hence, adequate decoupling and smoothing must be provided on the 5V. Excess ripple & noise may degrade the performance of the module.

4.8 INTERNAL AJUSTMENT POINTS:

Drawing showing internal Adjustment points and TX power link on the LC.



Drawing showing internal adjustments and TX power link on the LRT.



4.8.1 MODULATION BALANCE:

This is factory set and should not be adjusted; accept by qualified personnel in conjunction with the alignment manual and suitable test equipment. Changes may effect the quality of the modulated signal.

4.8.2 RF POWER LEVEL

The RF power level can be set internally, by the preset potentiometer, as indicated on the above drawing, or externally via a control voltage in the range 0-5Volts. The input goes via an internal low pass filter, making it suitable to control with PWM.

4.8.2.1 Internal Preset Power Link

For internal preset operation a 0805 Zero ohm resistor or wire link should be fitted as shown on the drawing above. For external TX power control the link should be omitted.

4.8.2.2 TX Power Timing

The timing for the TX power control is explained in the "Sequence to Raise the Transmitter" in the Synthesizer loading section.

4.8.3 MUTE LEVEL

The mute level is normally factory adjusted for a 12dB SINAD point. However, this can be changed by connecting a signal generator on the operating frequency to the antenna socket and adjusting the preset to the required level.

4.8.4 FREQUENCY ADJUSTMENT

Because the 5Volt supply may vary from client to client and hence the voltage on the TX AUD (DC Modulation point) will also vary, it is important that once the LC or LRT is operational on the PCB the final frequency should be trimmed.
To set the Frequency simply activate the transmitter on any channel, measure the frequency with a suitable frequency counter and adjust the "Frequency Trimming" point through the hole in the lid of the module. This will trim the receiver and all operational channels at the same time.

4.9 SYNTHESIZER LOADING & TX ENABLE SEQUENCE

These notes should be read in conjunction with the National Semiconductors data sheet on the LMX2316.

The synthesiser is loaded in two parts. The first time the synthesiser is loaded it should be loaded in Fast Lock mode #1 with the N counter 'GO' bit (N19) set to 1. Upon receipt of the lock signal, the synthesiser should be reloaded with the N19 bit zero (charge pump =250uA).
The function latches should be set as follows:

C 1	C 2	F 1	F 2	F 3	F 4	F 5	F 6	F 7	F 8	F 9	F 10	F 11	F 12	F 13	F 14	F 15	F 16	F 17	F 18
1	1	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

bits	function
C1-C2	Function latch address 11 selects "initialisation sequence method" (see LMX2316 data sheet).
F1	Counter reset not required using "initialisation sequence method"
F2	Power down off
F3-F5	Fo/LD mode set to "digital lock detect"
F6	Phase detector polarity positive
F7	Charge pump operation normal
F8--F10	Fastlock mode #1
F11-F14	Timeout counter 3 cycles (not used)
F15-F17	Test modes all off
F18	Power down off

4.9.1 TX & RX ENABLE SEQUENCE

The following Transmitter and Receiver enable sequence should be followed: -

1. The TX VCO should be enabled by putting TXSH low.

2. The synthesiser should be loaded in fast lock mode (N19 GO bit = 1). The sequence used for loading should be 1) function latches 2) reference divider 3) N counter.

3. Upon a successful lock signal, the N counter should be reloaded in normal mode (Go bit = 0). The function latches and reference divider should not be reloaded.

4. After rechecking the lock signal, the pin diode antenna switch should be operated via PTT. The pin diode switch should be in the transmit mode 1 to 2 milliseconds before TXP is enabled.

5. When returning to receive from transmit TXP must be set to 0V first, the pin diode switch (PTT) should be returned to the receive mode 3 to 6 milliseconds after TXP has been released to allow the transmit power time to drop.

6. Enable the RX VCO by putting TXSH high.

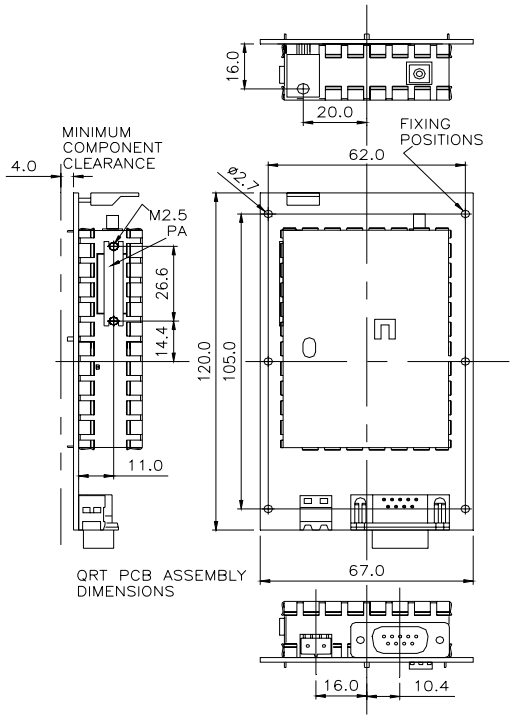
7. Reload the synthesizer for receive using the same sequence as described in steps 2 and 3. Note, for UHF the RX frequency loaded should be RX – 45MHz and for VHF it should be RX + 45MHz.

4.10 PIC PROCESSORS WITH MODEM SOFTWARE

Two Modem PIC processor are available to control the radio and provide modem functions. The only difference between them is maximum over the air data rate. The PICM1 has a maximum FFSK speed of 2400 while the PICM2 operates with GMSK up to 4800bps.
Control information is shown in section 7.

4.11 QRT SERIES CONTROL & INTERFACE PCB's

The control & interface boards within our QRT range of products support both the LC & LRT modules and are available for incorporation into clients equipment or as complete QRT product. Further details can be found in the QRT leaflet & manual.



4.11.2 QRT RS232 RADIO MODEM PCB

The RS323 QRT pcb is an RS232 Radio modem with a programmable baud rate of 150 – 4800bps and a manual channel control, although the channel and other features can be changed via the MPU interface. The PCB has a "D" interface and can take either the LC or LRT module. The product can be supplied as a transceiver, transmitter or receiver

4.11.3 QRT 5V TTL & AUDIO PCB

The 5VTTL & Audio QRT pcb is available as a transceiver, transmitter or receiver , with and audio input/output and access to a 150-2400bps modem via a 5VTTK serial port

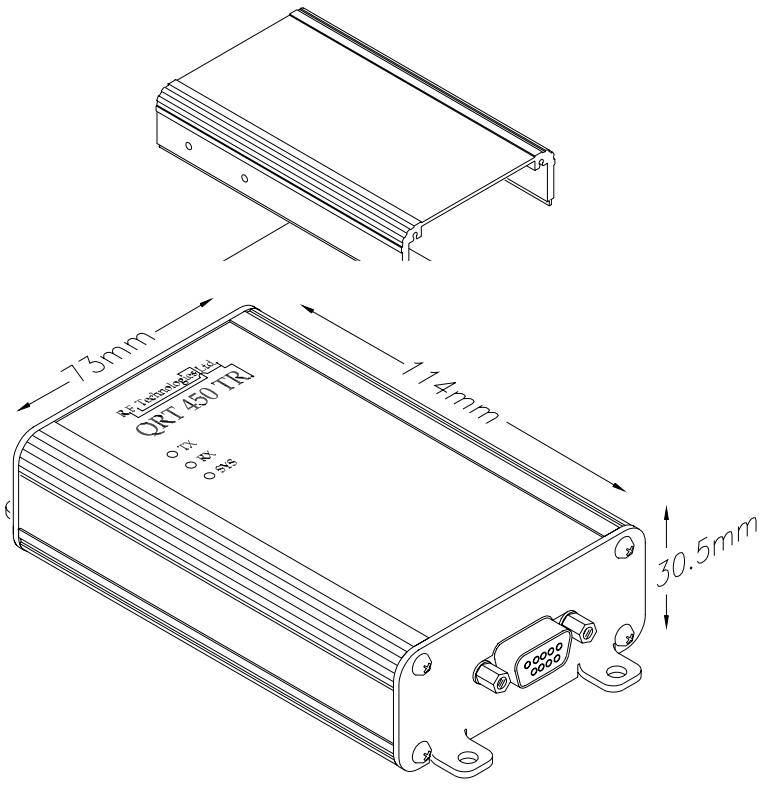
4.10.4 CUSTOM CONTROL & INTERFACE BOARDS

Custom control & interface boards can be designed for application specific product, further details can be obtained from our technical support staff.

4.11 QRT COMPLETE PRODUCT

Should a stand alone product be required with the LC/LRT & RS232 or Audio/TTL PCB and fitted into an enclosure, then the it can be purchased in the form of a QRT

Note: The enclosure can be purchased in varying sizes for use in clients own designs.



5.1 PIC CONTROLLER SOFTWARE

As a guide section 5.0 lists PIC code suitable to control the LC & LRT, Alternatively pre-programmed PIC microprocessor controllers can be ordered from the sales office.

5.2 EXAMPLE OF PIC SOFTWARE

```
THE CODE BELOW IS USED TO LOAD THE 2316 SYNTHESISER IN A PIC16F876, THE PORT PINS ARE
DEFINED AS FOLLOWS:

SCK             EQU 0x05        ;SERIAL BUS CLOCK OUTPUT ON PORT A
SD              EQU 0x02        ;SERIAL BUS DATA OUTPUT ON PORT A

RADEN           EQU 0x00        ;RADIO ENABLE OUTPUT ON PORT B

SLOCK           EQU 0x05        ;SYNTHESISER LOCK INPUT ON PORT C (HIGH=LOCKED)
TXSHIFT         EQU 0x04        ;TX SHIFT OUTPUT ON PORT C (I/P IF RX/TX ONLY)
PLLCS           EQU 0x03        ;PLL STOBE OUTPUT ON PORT C

THE REGISTER DEFINITIONS ARE AS FOLLOWS, THE CFG0-CFG4 LOCATIONS ARE PART OF
THE CONFIG DATA DOWNLOADED FROM EEPROM ON POWER UP, FOR AN OPERATING FREQUENCY
OF 458.5MHz CFG0 TO CFG4 WOULD CONTAIN THE HEX VALUES  DE, 90, C2, 70, 41,
RESPECTIVELY:

CFG0            EQU 0x30
CFG1            EQU 0x31
CFG2            EQU 0x32
CFG3            EQU 0x33
CFG4            EQU 0x34

TXPLL0          EQU CFG0        ;TX SYNTHESISER CODE MSB
TXPLL1          EQU CFG1        ;TX SYNTHESISER CODE LSB
RXPLL0          EQU CFG2        ;RX SYNTHESISER CODE MSB
RXPLL1          EQU CFG3        ;RX SYNTHESISER CODE LSB
```

```
SOFSET          EQU CFG4        ;SYNTHESISER OFFSET MSB, CHANNEL RESOLUTION.

PLFLGS          EQU 0x40        ;PLL COPY OF FFSKFLGS
PLSHF0          EQU 0x41        ;PLL SHIFT REGISTER MSB
PLSHF1          EQU 0x42        ;PLL SHIFT REGISTER
PLSHF2          EQU 0x43        ;PLL SHIFT REGISTER LSB
PLSTK0          EQU 0x44        ;PLL STACK
PLSTK1          EQU 0x45        ;PLL STACK
PLSTK2          EQU 0x46        ;PLL STACK
;*******************************************************************************
;THE PLLLOAD ROUTINES LOAD THE NATIONAL 2306 RADIO SYNTHESISER. THE SYNTHESISER
;REQUIRES A 21 BIT SHIFT, THE FIRST 19 BITS ARE DATA, THE LAST TWO ARE ADDRESS.
;THE DATA IS SHIFTED MSB FIRST. TAKING THE CONVENTION THAT THE TWO LSB OF THE
;SHIFTED WORD ARE ADDRESS (A1,A0) AND THE 19 MSB ARE DATA (D18-D0) ADDRESSES TO
;BE LOADED ARE:
;
;       0       REFERENCE DIVIDER       D0-D13 DIVIDE RATIO
;                                       D14-D17 TEST MODES (MUST BE ZERO)
;                                       D18 LD PRECISION
;       1       MAIN DIVIDER            D0-D2,D5-D17 DIVIDE RATIO (D3,D4 DEAD)
;                                       D18 GO BIT
;       2/3     CONTROL REGISTER        D0 COUNTER RESET
;                                       D1 POWER DOWN
;                                       D2-D4 Fo/LD
;                                       D5 PHASE DETECTOR POLARITY
;                                       D6 CP TRI-STATE
;                                       D7-D9 FASTLOCK MODES
;                                       D10-D13 TIMEOUT COUNTER
;                                       D14-16 TEST MODES (MUST BE ZERO)
;                                       D17 POWER DOWN MODE
;                                       D18 TEST MODE (MUST BE ZERO)
;

;THE ADDRESS USED TO PROGRAM THE CONTROL REGISTER AFFECTS THE WAY THE CHIP
;STARTS UP, ADDRESS 3 IS USED. THE ORDER OF LOADING USED IS ALSO IMPORTANT,
;THE SEQUENCE CONTROL, REFERENCE, MAIN IS USED.
;

;THE REFERENCE DIVIDER RATIO IS CALCULATED AS OSC/REF = 12.6MHz/6.25kHz = 2016.
;THE MAIN DIVIDER RATIO IS CALCULATED AS F/REF WHICH CAN BE EXPRESSED IN 17
;BITS, THIS VALUE IS HELD IN THE TXPLL REGISTERS, THE REMAINING MS BIT IS SET
;TO ZERO. WHEN LOADING THE S40,41,42 REGISTERS THE DATA MUST BE LEFT JUSTIFIED
;WHERE S40 IS THE MSB, THE ADDRESS BITS ARE THEREFORE LOADED TO S42 BITS 4 AND
;3.
;
;THE 17 BIT PLL DATA IS PASSED TO THIS ROUTINE IN THREE REGISTERS, THE FIRST OF
;WHICH IS POINTED BY S28 EG RXPLL0 TO 2 (POINTED AS RXPLL0) OR TXPLL0 TO 2
;(POINTED AS TXPLL0), RX/TXPLL0 CONTAINS THE 17TH PLL BIT IN BIT 0, THE
;REMAINING TWO BYTES CONTAIN THE OTHER 16 BITS. HAVING LOADED THE PLL CHIP
;SYNTHESISER LOCK IS WAITED UPON, IF THIS DOES NOT OCCURR WITHIN 250MS THE
;ERROR ROUTINE IS JUMPED TO. NOTE THAT BEFORE WAITING FOR LOCK THE ROUTINE
;WAITS 15MS FOR THE SYNTHESISER TO UNLOCK.
;
;RX PLL VALUE FOR UHF IS GIVEN BY (F-45MHZ)/REF, FOR TX IT IS F/REF.
;
;FOR 6.25kHz REF THE REFERENCE CODE IS 07E0H, FOR 5.0kHz THE CODE IS 09D8.
;THESE CODES ARE LOADED SHIFTED THREE BITS RIGHT, THE CODES THEREFORE BECOME
;00FCH AND 013BH, NOTE THAT NO BITS ARE SHIFTED OUT OF THE LSB AND SO A FURTHER
;BYTE IS NOT REQUIRED.
;
;IN ORDER TO ALLOW PLL CODES TO BE STORED IN 16 BITS AN OFFSET OF 4000 HEX IS
;ADDED TO THE PLL CODES HERE TO ACHEIVE THE FINAL CODE. THIS ALLOWS A FREQUENCY
;RANGE OF 102.4 TO 511.99375MHz TO BE LOADED.

REFH6           EQU 000H        ;6.25 REFERENCE
REFL6           EQU 0FCH
REFH5           EQU 001H        ;5.00 REFERENCE
REFL5           EQU 03BH

PLLLOAD:BSF PCLATH,0x03
        CALL PORTADIG           ;CHANGE PORT A TO ALL DIGITAL.
        CLRF PCLATH

        CLRF CCP1CON            ;STOP PWM POWER CONTROL,

        BCF FFSKFLGS,EDEN       ;DISABLE DECODER AND ENCODER TO ALLOW PLL
                                ;REGISTER USE.
        MOVF PORTB,W            ;FETCH A COPY OF PORT B,
        MOVWF PLFLGS            ;TRANSFER TO PLL FLAGS.
        BCF PORTB,RADEN         ;POWER UP RADIO,
        BTFSS PLFLGS,RADEN      ;WAS RADIO PREVIOUSLY ENABLED ?
        GOTO PLLL1              ;IF NOT THIS IS A POWER UP LOAD.
        MOVLW 10                ;WAIT 5 MILLISECS FOR RF MODULE TO STABILISE.
        CALL PLWAIT
```

```
PLLL1:  MOVLW TXPLL0          ;SET W TO POINT AT TX PLL REGISTERS,
        BTFSS PSTAT,TXON
        MOVLW RXPLL0          ;IF RX LOAD SET W TO POINT AT RX PLL REGISTERS,
        MOVWF FSR             ;LOAD POINTER TO FSR.
        BCF STATUS,IRP

        BCF PORTA,SD          ;INITIALISE PLL LINES.
        NOP
        BCF PORTA,SCK
        NOP
        BSF PORTC,PLLCS

        MOVLW 00000000B       ;TEST MODES ALL 0, POWER DOWN MODE 0, TIMEOUT
        MOVWF PLSHF0          ;COUNTER ZERO (3 PD CYCLE TIMEOUT), FAST LOCK
        MOVLW 00010100B       ;MODE 1, CP TRI-STATE 0, PHASE DETECTOR
        MOVWF PLSHF1          ;POLARITY 1, DIGITAL LOCK DETECT, POWER DOWN 0,
        MOVLW 10011000B       ;COUNTER RESET 1. ADDRESS 3.
        MOVWF PLSHF2
        CALL PLLSHIFT

        MOVLW REFH6           ;THE CONSTANTS USED TO LOAD THE REFERENCE ARE
        BTFSS SOFSET,0x00     ;ALREADY ALIGNED CORRECTLY, THE REF LSB SHOULD
        MOVLW REFH5           ;ACTUALLY BE IN PLSHF2 BITS 5,6,7, HOWEVER
        MOVWF PLSHF0          ;THESE THREE BITS ARE ZERO FOR EITHER REFERENCE
        MOVLW REFL6           ;FREQUENCY AND SO DO NOT NEED LOADING.
        BTFSS SOFSET,0x00
        MOVLW REFL5           ;LD PRECISION AND TEST MODE BITS ARE ALL ZERO.
        MOVWF PLSHF1          ;ADDRESS IS ALSO ZERO.
        CLRF PLSHF2
        CALL PLLSHIFT

        CLRF PLSHF0
        MOVF SOFSET,W         ;LOAD POINTED REGISTERS TO PLL SHIFT REGISTERS,
        ANDLW 0xFC            ;ADD OFFSET TO HIGH BYTE MAKING SURE FLAGS IN
        ADDWF IND,W           ;BITS 0,1 DELETED. BIT17 GENERATED IN CARRY.
        RLF PLSHF0
        MOVWF PLSHF1
        INCF FSR,F
        MOVF IND,W
        MOVWF PLSHF2
        MOVLW 5               ;ALIGN CODE SO ITS LSB IS IN PLSHF2 BIT 5,
        MOVWF S0
PLL4:   BCF STATUS,CARRY      ;CLEAR CARRY SO THAT ADDRESS BITS END UP ZERO,
        RLF PLSHF2
        RLF PLSHF1
        RLF PLSHF0
        DECFSZ S0
        GOTO PLL4
        BSF PLSHF2,003H       ;SET ADDRESS TO ONE,
        BSF PLSHF0,007H       ;AND SET GO BIT.
        MOVF PLSHF0,W         ;SAVE CODES SO GO BIT CAN BE CLEARED EASILY
        MOVWF PLSTK0          ;LATER.
        MOVF PLSHF1,W
        MOVWF PLSTK1
        MOVF PLSHF2,W
        MOVWF PLSTK2
        CALL PLLSHIFT

        CLRF PLSHF0           ;PLSHF0 AND 1 ARE USED TO TIME WAIT FOR LOCK.
        CLRF PLSHF1
        BCF PSTAT,ERRUNLK     ;CLEAR THE UNLOCK FLAG,
PLL1:   CLRWDT                ;CLEAR WATCHDOG,
        BTFSC PORTC,SLOCK     ;EACH PASS OF DECFSZ PLSHF0 TAKES ABOUT 6us
        GOTO PLL3             ;SO 65536 PASSES TAKE ABOUT 390ms.
        DECFSZ PLSHF0
        GOTO PLL1
        DECFSZ PLSHF1
        GOTO PLL1
        BSF PSTAT,ERRUNLK     ;IF TIMEOUT OCURRS SET ERROR FLAG AND EXIT.
        GOTO PLL5

PLL3:   MOVLW 4               ;WAIT 2MS,
        CALL PLWAIT
        BTFSS PORTC,SLOCK     ;ARE WE STILL LOCKED ?
        GOTO PLL1             ;IF NOT RE-ENTER LOOP.

        MOVF PLSTK0,W         ;RETRIEVE LAST PLSHF VALUES,
        MOVWF PLSHF0
        MOVF PLSTK1,W
        MOVWF PLSHF1
        MOVF PLSTK2,W
        MOVWF PLSHF2
        BCF PLSHF0,007H       ;CLEAR THE GO BIT TO STOP FAST LOCK.
        CALL PLLSHIFT
```

```
PLL5:   BSF PCLATH,0x03
        CALL PORTAAN            ;RESTORE PORT A TO ANALOGUE OPERATION.
        CLRF PCLATH
        RETURN                  ;EXIT.

PLLSHIFT:
        BCF PORTA,SCK           ;MAKE SURE CLOCK STARTS LOW.
        NOP
        BCF PORTC,PLLCS         ;SET CHIP SELECT LOW,
        MOVLW 21                ;S0 COUNTS 21 SHIFTS,
        MOVWF S0

PLLS2:  BTFSC PLSHF0,007H       ;SET DATA LINE ACCORDING TO PLSHF0 MSB,
        GOTO PLLS1
        BCF PORTA,SD
        GOTO PLLS3
PLLS1:  BSF PORTA,SD
        NOP
PLLS3:  BSF PORTA,SCK           ;OPERATE CLOCK,
        BCF PORTA,SCK
        RLF PLSHF2              ;SHIFT NEXT BIT INTO PLSHF0 BIT 7,
        RLF PLSHF1
        RLF PLSHF0
        DECFSZ S0
        GOTO PLLS2

        BSF PORTC,PLLCS         ;DESELECT PLL,
        RETURN

;*************************************************************************
;PLWAIT WAITS FOR 0.5ms TIMES THE VALUE PASSED IN W. NOTE THAT THE CLOCK
;REGISTERS ARE CORRUPTED WHEN THIS ROUTINE IS USED FOR GREATER ACCURACY.

PLWAIT: MOVWF S1                ;SAVE PASSED VALUE IN S1.
        MOVF S1,W
        BTFSC STATUS,ZFLG       ;IF ZERO JUST EXIT.
        GOTO PLW3
PLW2:   CLRWDT
        MOVLW 10                ;SET CLOCK PRESCALER FOR 0.5ms TIMEOUT,
        MOVWF CKPRE
        MOVLW 0x10              ;LOAD SOME ARBITRARY VALUE TO SECONDS PRESCALER
        MOVWF SECPRE            ;AND WAIT FOR IT TO CHANGE,
PLW1:   BTFSC SECPRE,0x04
        GOTO PLW1
        DECFSZ S1               ;DECREMENT LOOP COUNT UNTIL ZERO.
        GOTO PLW2
PLW3:   RETURN
```

6.1. PIC MODEM INTERFACE PROTOCOL (Version A Aug 00)

The LRT/LC PIC processor was designed to communicate with an Intel 8051 UART running in mode 3. Mode 3 on the 8051 is an 11 bit asynchronous mode. Communications are run at 9600 baud. Each serial character consists of a start bit, 8 data bits, a ninth programmable bit and a stop bit. The ninth programmable bit is used as a control flag to differentiate between control functions and data. Only two connections are required to the host, TXD and RXD, where TXD is serial data going into the PIC and RXD is that coming out (a common ground connection is assumed).

Because of limited buffer size all characters passed to the radio PIC will be subject to a data/ack handshake process, the ACK character is returned following every character to indicate that the device is ready to accept the next character. This applies to both data and control characters. In the case where control data is requested from the radio PIC using the ENQ command the ACK character is replaced by the RQD character, this character denotes that the following data byte is requested control data and not receive data, in this case the PIC may not be considered to be ready for another character until both bytes have been output.

The radio PIC may be put into sleep mode at the command of the host using the SLEEP control character, it is woken up by using the WAKE character, note that receipt of any character will actually wake up the PIC however the device will not be able to interpret characters received in sleep mode, the device therefore assumes that any character received while in sleep mode is a

WAKE character. To avoid possible framing errors during waking the WAKE character is specially chosen such that it consists of all ones, the only signal seen is therefore a single start bit. If in error the host sends a command to the PIC while the device is asleep there is a possibility that the acknowledgement returned on waking is mistaken for acceptance of the command that woke the device, for this reason a special WAKAK character is reserved for use as an acknowledgement only for wake up. Receipt of this character in response to any command other than WAKE should be deemed as an error.

The radio PIC is half duplex and so must suspend receive operations if passed transmit data. Data passed for transmission is considered to be a higher priority. If the PIC is passed a transmit start instruction (TXSTT) it will discard the contents of its receiver buffer although it will complete the output of any character currently in progress. The transmit buffer is limited in size to one character and so a serial handshake procedure is used for flow control, receipt of any character for transmission will result in a ACK control character being returned indicating that the device is ready for another data character. If no more data is to be sent the TXEND control character may be sent to tell the PIC to suspend transmit mode and return to receive. In this case the ACK character will be returned to confirm that the device has completed transmission of all data and has returned to receive.

The CFG control character allows configuration parameters to be passed, these parameters will be passed as two bytes where the second byte is the configuration parameter and is a data character (i.e. the control bit is not set), the CFG character is used to tell the radio PIC that the next character will be a configuration parameter and not data intended for transmission. The lower 5 bits of the CFG character also contains an address (0 to 31) to tell the radio PIC where to put the parameter, the device will not verify the legality of the parameter, this process may therefore be considered as a low level 'poke' access.

The ENQ character allows control data to be read from the radio, this is the 'peek' counterpart to the CFG character. The lower 5 bits of the ENQ character contain the address from which data is requested. The response to this request will be the RQD character followed by the requested data.

Data that may be requested from the radio is as follows:

Status byte: (address 0) Returns 8 bits as follows

bit 0 1 = channel busy
bit 1 1 = data carrier detected
bit 2 1 = transmitter on
bit 3 1 = test mode on
bit 4 1 = synthesiser out of lock
bit 5 1 = rx buffer overflow
bit 6 1 = tx buffer overflow
bit 7 1 = power on reset status

bits 4 to 7 are all error conditions, power on reset status will be assumed at power on and as a result of a watchdog reset on the radio.

Type: (address 1) Returns an 8 bit identifier to signify the radio type e.g. UHF MPT1329.

Version: (address 2) Returns the code version running in the radio.

The TEST character allows the radio PIC to be put into a test mode, the lower 6 bits of the character denote the test number to be run, passing a test number of zero restores normal operation.

Tests that may be run for the radio are as follows;

Test 1 Transmit continuous zero tone
Test 2 Transmit continuous one tone
Test 3 Transmit continuous carrier
Test 4 Transmit 50Hz square wave

The control characters are shown below:

NAME	BINARY	SOURCE
CFG	1,000a,aaaa, 0,dddd,dddd	HOST (a=address, d=data)
TXEND	1,0010,0000	HOST
ENQ	1,010a,aaaa	HOST (a=address)
TEST	1,011n,nnnn	HOST
SLEEP	1,1000,0000	HOST
TXSTT	1,101d,dddd	HOST (d=lead in delay)
WAKE	1,1111,1111	HOST
ACK	1,0000,0000	COMMS
RQD	1,0000,0001, 0,dddd,dddd	COMMS (d=data)
WAKAK	1,0000,0010	COMMS

Lead in delay is passed in the 5 lsb of the TXSTT command as follows, if bit 4 is not set bits 0-3 give the lead in delay multiplied by 5ms (0-75ms), if bit 4 is set bits 0-3 give the lead in delay multiplied by 80ms (0-1200ms). The lead in delay is the amount of time that the transmitter is raised prior to sending data, for the LPR450 radio this delay should be at least 40ms.

Configuration parameters for the radio are shown below:

NAME	ADDRESS	FUNCTION
TXPLL0	00	msd of the synthesiser TX code
TXPLL1	01	lsd of the synthesiser TX code
RXPLL0	02	msd of the synthesiser RX code
RXPLL1	03	lsd of the synthesiser RX code
OFFSET	04	synthesiser offset
FFBAUD	05	sets FFSK baud rate as follows
		bit 0 1=1200 baud
		bit 1 1=600 baud
		bit 2 1=300 baud
		bit 3 1=600 baud
		bit 4 not used
		bit 5 not used
		bit 6 not used
		bit 7 1=2400 baud
FFMODE	06	sets FFSK format as follows
		bit 0 not used
		bit 1 not used

bit 2	not used
bit 3	not used
bit 4	1=7 bit, 0=8 bit
bit 5	1=parity on, 0=off
bit 6	1=odd parity, 0=even
bit 7	1=two stop bits, 0=one

Synthesiser divider values are calculated as follows:

TX divider = TX frequency in Hertz / 6250

RX divider = (RX frequency in Hertz + I.F. frequency in Hertz) / 6250

N.B. the I.F. frequency can be positive or negative

e.g. for a UHF radio the I.F. frequency is -45MHz. Therefore for RX and TX frequencies of 458.5 MHz the TX divider is 73360 (11E90 hex) and the RX divider value is 66160 (10270 hex).

For a band 1 radio the I.F. frequency is +21.4MHz. Therefore for RX and TX frequencies of 45 MHz the TX divider is 7200 (1C20 hex) and the RX divider is 10624 (2980 hex).

The OFFSET parameter is used to reduce the size of synthesiser RX and TX codes to 16 bit values if necessary, for the above UHF example an offset of 4000 hex is chosen, the offset value must be exactly divisible by 256 as only the m.s. byte is loaded to the PIC, thus for an offset of 4000 hex the value 40 hex is loaded as the parameter OFFSET and the synthesiser codes have 4000 hex subtracted from them to become TX code DE90 hex and RX code C270 hex. For the above band 1 example the divider values can both be represented within 16 bits and so an offset of zero can be used, the OFFSET value would therefore be 00 hex, the TX code 1C20 hex, and the RX code 2980 hex.

All 7 configuration parameters MUST be loaded to the radio in the order CFG0 to CFG6, individual parameters cannot be changed without re-writing all of the remaining parameters, if incomplete configuration writes are performed the power on reset status flag will become set and remain set, the radio will not then operate until a complete configuration write is done.

EXAMPLES

Below are shown the word sequences for various functions as seen on the TXD and RXD lines of the radio PIC. The hex values of the 9 bit words are shown along with their mnemonics.

1/ Configuration of the radio for TX and RX frequencies of 458.5MHz, 1200 baud comms with format 8 bits, no parity, 1 stop bit.

	TXD	RXD	
CFG0	100		
		100	ACK
TXPLL0 config byte	0DE		
		100	ACK
CFG1	101		
		100	ACK
TXPLL1 config byte	090		
		100	ACK
CFG2	102		
		100	ACK

RXPLL0 config byte	0C2		
		100	ACK
CFG3	103		
		100	ACK
RXPLL1 config byte	070		
		100	ACK
CFG4	104		
		100	ACK
OFFSET config byte	040		
		100	ACK
CFG5	105		
		100	ACK
FFBAUD config byte	001		
		100	ACK
CFG6	106		
		100	ACK
FFMODE config byte	000		
		100	ACK

2/ A status request.

	TXD	RXD	
ENQ0	140		
		101	RQD
		001	status

3/ Start transmitter with 40ms lead in delay, transmit the characters ABC, and then stop the transmitter.

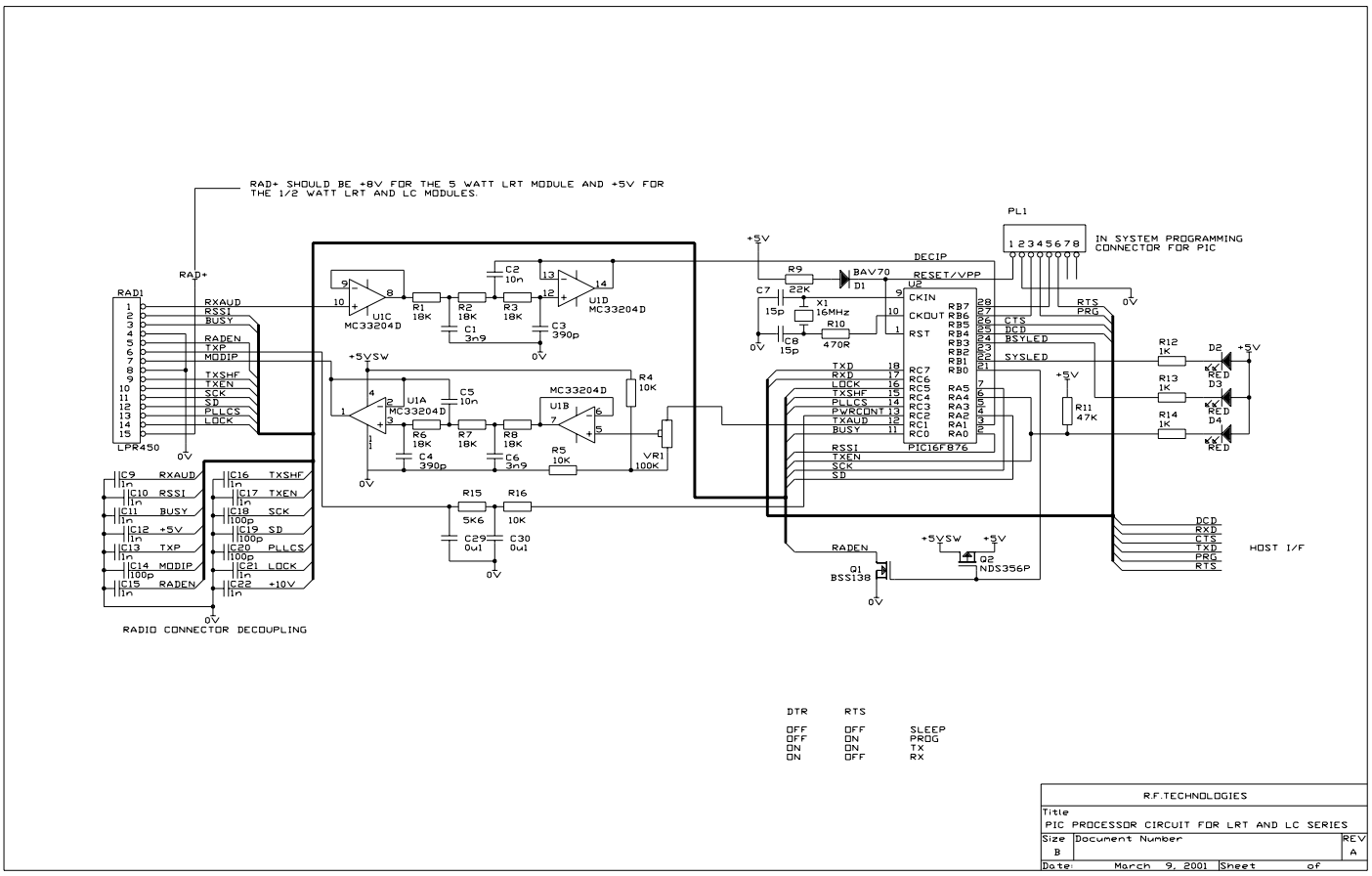
	TXD	RXD	
TXSTT (lid=40ms)	1A8		
		100	ACK
ascii A	041		
		100	ACK
ascii B	042		
		100	ACK
ascii C	043		
		100	ACK
TXEND	120		
		100	ACK

4/ Receiving the characters ABC

	TXD	RXD	
		041	ascii A
		042	ascii B
		043	ascii C

5/ Putting the radio to sleep and then waking it up.

	TXD	RXD	
SLEEP	180		
		100	ACK
WAKE	1FF		



7.0 INTERFACE CIRCUIT

The circuit above is a typical interface circuit for connecting an LC or LRT to a PIC MPU with U1A & U1B providing necessary filtering for the TX path and U1C/UID filtering the received audio signal.
PWM is used for the RF power control with filtering provided by R15,16 and C29,30.

The PIC complete with modem code an be purchased from the sales office.